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Correctness of Binary Counter Circuits

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Summary. This article introduces the verification of the correctness for the operations and the specification of the 3-bit counter. Both cases: without reset input and with reset input are considered. The proof was proposed by Y. Nakamura in [1].

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The article [1] provides the notation and terminology for this paper.

In this paper a, b, c, d denote sets.

We now state four propositions:

(1) Let s_0, s_1, s_2, s_3, s_4, s_5, s_6, s_7, n_0, n_4, n_5, n_6, n_7, n_8, n_9, n_{10}, q_1, q_2, q_3, n_1, n_2, n_3 be sets such that NE s_0 iff NE AND3(NOT1 q_3, NOT1 q_2, NOT1 q_1) and NE s_1 iff NE AND3(NOT1 q_3, NOT1 q_2, q_1) and NE s_2 iff NE AND3(NOT1 q_3, q_2, NOT1 q_1) and NE s_3 iff NE AND3(NOT1 q_3, q_2, q_1) and NE s_4 iff NE AND3(q_3, NOT1 q_2, NOT1 q_1) and NE s_5 iff NE AND3(q_3, NOT1 q_2, q_1) and NE s_6 iff NE AND3(q_3, q_2, NOT1 q_1) and NE s_7 iff NE AND3(q_3, q_2, q_1) and NE n_0 iff NE AND3(NOT1 n_3, NOT1 n_2, NOT1 n_1) and NE n_4 iff NE AND3(NOT1 n_3, NOT1 n_2, n_1) and NE n_5 iff NE AND3(NOT1 n_3, n_2, NOT1 n_1) and NE n_6 iff NE AND3(NOT1 n_3, n_2, n_1) and NE n_7 iff NE AND3(n_3, NOT1 n_2, NOT1 n_1) and NE n_8 iff NE AND3(n_3, NOT1 n_2, n_1) and NE n_9 iff NE AND3(n_3, n_2, NOT1 n_1) and NE n_{10} iff NE AND3(n_3, n_2, n_1) and NE n_1 iff NE NOT1 q_1 and NE n_2 iff NE XOR2(q_1, q_2) and NE n_3 iff NE OR2(AND2(q_3, NOT1 q_1), AND2(q_1, XOR2(q_2, q_3))). Then

(i) NE n_4 iff NE s_0,

(ii) NE n_5 iff NE s_1,

(iii) NE n_6 iff NE s_2,

(iv) NE n_7 iff NE s_3,

(v) NE n_8 iff NE s_4,

(vi) NE n_9 iff NE s_5,

(vii) NE n_{10} iff NE s_6, and

(viii) NE n_0 iff NE s_7.

(2) NE AND3(AND2(a, d), AND2(b, d), AND2(c, d)) iff NE AND2(AND3(a, b, c), d).

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(3)(i) Not NE AND2(a,b) iff NE OR2$(\mathrm{NOT1}\,a,\mathrm{NOT1}\,b)$,

(ii) NE OR2(a,b) and NE OR2(c,b) iff NE OR2$(\mathrm{AND2}(a,c),b)$,

(iii) NE OR2(a,b) and NE OR2(c,b) and NE OR2(d,b) iff NE OR2$(\mathrm{AND3}(a,c,d),b)$, and

(iv) if NE OR2(a,b) and NE a iff NE c, then NE OR2(c,b).

(4) Let s_0, s_1, s_2, s_3, s_4, s_5, s_6, s_7, n_0, n_4, n_5, n_6, n_7, n_8, n_9, n_{10}, q_1, q_2, q_3, n_1, n_2, n_3, R be sets such that NE s_0 iff NE AND3$(\mathrm{NOT1}\,q_3,\mathrm{NOT1}\,q_2,\mathrm{NOT1}\,q_1)$ and NE s_1 iff NE AND3$(\mathrm{NOT1}\,q_3,\mathrm{NOT1}\,q_2,q_1)$ and NE s_2 iff NE AND3$(\mathrm{NOT1}\,q_3,q_2,\mathrm{NOT1}\,q_1)$ and NE s_3 iff NE AND3$(\mathrm{NOT1}\,q_3,q_2,q_1)$ and NE s_4 iff NE AND3$(q_3,\mathrm{NOT1}\,q_2,\mathrm{NOT1}\,q_1)$ and NE s_5 iff NE AND3$(q_3,\mathrm{NOT1}\,q_2,q_1)$ and NE s_6 iff NE AND3$(q_3,q_2,\mathrm{NOT1}\,q_1)$ and NE s_7 iff NE AND3(q_3,q_2,q_1) and NE n_0 iff NE AND3$(\mathrm{NOT1}\,n_3,\mathrm{NOT1}\,n_2,\mathrm{NOT1}\,n_1)$ and NE n_4 iff NE AND3$(\mathrm{NOT1}\,n_3,\mathrm{NOT1}\,n_2,n_1)$ and NE n_5 iff NE AND3$(\mathrm{NOT1}\,n_3,n_2,\mathrm{NOT1}\,n_1)$ and NE n_6 iff NE AND3$(\mathrm{NOT1}\,n_3,n_2,n_1)$ and NE n_7 iff NE AND3$(n_3,\mathrm{NOT1}\,n_2,\mathrm{NOT1}\,n_1)$ and NE n_8 iff NE AND3$(n_3,\mathrm{NOT1}\,n_2,n_1)$ and NE n_9 iff NE AND3$(n_3,n_2,\mathrm{NOT1}\,n_1)$ and NE n_{10} iff NE AND3(n_3,n_2,n_1) and NE n_1 iff NE AND2$(\mathrm{NOT1}\,q_1,R)$ and NE n_2 iff NE AND2$(\mathrm{XOR2}(q_1,q_2),R)$ and NE n_3 iff NE AND2$(\mathrm{OR2}(\mathrm{AND2}(q_3,\mathrm{NOT1}\,q_1),\mathrm{AND2}(q_1,\mathrm{XOR2}(q_2,q_3))),R)$. Then

(i) NE n_4 iff NE AND2(s_0,R),

(ii) NE n_5 iff NE AND2(s_1,R),

(iii) NE n_6 iff NE AND2(s_2,R),

(iv) NE n_7 iff NE AND2(s_3,R),

(v) NE n_8 iff NE AND2(s_4,R),

(vi) NE n_9 iff NE AND2(s_5,R),

(vii) NE n_{10} iff NE AND2(s_6,R), and

(viii) NE n_0 iff NE OR2$(s_7,\mathrm{NOT1}\,R)$.

REFERENCES

[1] Yatsuka Nakamura. Logic gates and logical equivalence of adders. *Journal of Formalized Mathematics*, 11, 1999. http://mizar.org/JFM/Vol11/gate_1.html.

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