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On the Composition of Macro Instructions of Standard Computers

Artur Korniłowicz
University of Białystok

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The articles [21], [27], [3], [4], [18], [14], [28], [9], [10], [20], [22], [8], [13], [23], [2], [5], [1], [6], [12], [11], [17], [7], [16], [24], [19], [25], [15], and [26] provide the notation and terminology for this paper.

1. PRELIMINARIES

We adopt the following rules: k, m are natural numbers, x, X are sets, and N is a set with non empty elements.

Let f be a function and let g be a non empty function. One can verify that $f{+}\cdot g$ is non empty and $g{+}\cdot f$ is non empty.

Let f, g be finite functions. One can check that $f{+}\cdot g$ is finite.

One can prove the following propositions:

(1) For all functions f, g holds $\operatorname{dom} f \approx \operatorname{dom} g$ iff $f \approx g$.

(2) For all finite functions f, g such that $\operatorname{dom} f$ misses $\operatorname{dom} g$ holds $\operatorname{card}(f{+}\cdot g) = \operatorname{card} f + \operatorname{card} g$.

Let f be a function and let A be a set. One can check that $f \setminus A$ is function-like and relation-like.

Next we state two propositions:

(3) For all functions f, g such that $x \in \operatorname{dom} f \setminus \operatorname{dom} g$ holds $(f \setminus g)(x) = f(x)$.

(4) For every non empty finite set F holds $\operatorname{card} F - 1 = \operatorname{card} F -' 1$.

2. PRODUCT LIKE SETS

Let S be a functional set. The functor $\prod_S$ yielding a function is defined by:

(Def. 1)(i) For every set x holds $x \in \operatorname{dom} \prod_S$ iff for every function f such that $f \in S$ holds $x \in \operatorname{dom} f$ and for every set i such that $i \in \operatorname{dom} \prod_S$ holds $\prod_S(i) = \pi_i S$ if S is non empty,

(ii) $\prod_S = \emptyset$, otherwise.

We now state two propositions:

(5) For every non empty functional set S holds $\operatorname{dom} \prod_S = \bigcap\{\operatorname{dom} f : f$ ranges over elements of $S\}$.

(6) For every non empty functional set S and for every set i such that $i \in \operatorname{dom} \prod_S$ holds $\prod_S(i) = \{f(i) : f$ ranges over elements of $S\}$.

Let S be a set. We say that S is product-like if and only if:

(Def. 2) There exists a function f such that $S = \prod f$.

Let f be a function. Observe that $\prod f$ is product-like.
Let us note that every set which is product-like is also functional and has common domain.
Let us note that there exists a set which is product-like and non empty.
The following propositions are true:

(7) For every functional set S with common domain holds $\operatorname{dom} \prod_S = \operatorname{DOM}(S)$.

(8) For every functional set S and for every set i such that $i \in \operatorname{dom} \prod_S$ holds $\prod_S(i) = \pi_i S$.

(9) For every functional set S with common domain holds $S \subseteq \prod \prod_S$.

(10) For every non empty product-like set S holds $S = \prod \prod_S$.

Let D be a set. One can verify that every set of finite sequences of D is functional.
Let i be a natural number and let D be a set. Observe that D^i has common domain.
Let i be a natural number and let D be a set. Note that D^i is product-like.

3. Properties of AMI-Struct

We now state two propositions:

(11) Let N be a set, S be an AMI over N, and F be a finite partial state of S. Then $F \setminus X$ is a finite partial state of S.

(12) Let S be an IC-Ins-separated definite non empty non void AMI over N and F be a programmed finite partial state of S. Then $F \setminus X$ is a programmed finite partial state of S.

Let N be a set with non empty elements, let S be an IC-Ins-separated definite non empty non void AMI over N, let i_1, i_2 be instruction-locations of S, and let I_1, I_2 be elements of the instructions of S. Then $[i_1 \longmapsto I_1, i_2 \longmapsto I_2]$ is a finite partial state of S.

Let N be a set with non empty elements and let S be a halting non void AMI over N. Note that there exists an instruction of S which is halting.

Next we state three propositions:

(13) Let S be a standard IC-Ins-separated definite non empty non void AMI over N, F be a lower programmed finite partial state of S, and G be a programmed finite partial state of S. If $\operatorname{dom} F = \operatorname{dom} G$, then G is lower.

(14) Let S be a standard IC-Ins-separated definite non empty non void AMI over N, F be a lower programmed finite partial state of S, and f be an instruction-location of S. If $f \in \operatorname{dom} F$, then $\operatorname{locnum}(f) < \operatorname{card} F$.

(15) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a lower programmed finite partial state of S. Then $\operatorname{dom} F = \{\operatorname{il}_S(k); k$ ranges over natural numbers: $k < \operatorname{card} F\}$.

Let N be a set, let S be an AMI over N, and let I be an element of the instructions of S. The functor AddressPart(I) is defined as follows:

(Def. 3) $\operatorname{AddressPart}(I) = I_{\mathbf{2}}$.

Let N be a set, let S be an AMI over N, and let I be an element of the instructions of S. Then AddressPart(I) is a finite sequence of elements of $\bigcup N \cup$ the carrier of S.

One can prove the following proposition

(16) Let N be a set, S be an AMI over N, and I, J be elements of the instructions of S. If $\mathrm{InsCode}(I) = \mathrm{InsCode}(J)$ and $\mathrm{AddressPart}(I) = \mathrm{AddressPart}(J)$, then $I = J$.

Let N be a set and let S be an AMI over N. We say that S is homogeneous if and only if:

(Def. 4) For all instructions I, J of S such that $\mathrm{InsCode}(I) = \mathrm{InsCode}(J)$ holds $\mathrm{dom}\,\mathrm{AddressPart}(I) = \mathrm{dom}\,\mathrm{AddressPart}(J)$.

The following proposition is true

(17) For every instruction I of $\mathrm{STC}(N)$ holds $\mathrm{AddressPart}(I) = 0$.

Let N be a set, let S be an AMI over N, and let T be an instruction type of S. The functor AddressParts T is defined as follows:

(Def. 5) $\mathrm{AddressParts}\,T = \{\mathrm{AddressPart}(I); I$ ranges over instructions of S: $\mathrm{InsCode}(I) = T\}$.

Let N be a set, let S be an AMI over N, and let T be an instruction type of S. Note that AddressParts T is functional.

Let N be a set with non empty elements, let S be an IC-Ins-separated definite non empty non void AMI over N, and let I be an instruction of S. We say that I has explicit jumps if and only if the condition (Def. 6) is satisfied.

(Def. 6) Let f be a set. Suppose $f \in \mathrm{JUMP}(I)$. Then there exists a set k such that $k \in \mathrm{dom}\,\mathrm{AddressPart}(I)$ and $f = (\mathrm{AddressPart}(I))(k)$ and $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(k) =$ the instruction locations of S.

We say that I has no implicit jumps if and only if the condition (Def. 7) is satisfied.

(Def. 7) Let f be a set. Given a set k such that $k \in \mathrm{dom}\,\mathrm{AddressPart}(I)$ and $f = (\mathrm{AddressPart}(I))(k)$ and $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(k) =$ the instruction locations of S. Then $f \in \mathrm{JUMP}(I)$.

Let N be a set with non empty elements and let S be an IC-Ins-separated definite non empty non void AMI over N. We say that S has explicit jumps if and only if:

(Def. 8) Every instruction of S has explicit jumps.

We say that S has no implicit jumps if and only if:

(Def. 9) Every instruction of S has no implicit jumps.

Let N be a set and let S be an AMI over N. We say that S has non trivial instruction locations if and only if:

(Def. 10) The instruction locations of S are non trivial.

Let N be a set with non empty elements. Note that every IC-Ins-separated definite non empty non void AMI over N which is standard has also non trivial instruction locations.

Let N be a set with non empty elements. Observe that there exists an IC-Ins-separated definite non empty non void AMI over N which is standard.

Let N be a set with non empty elements and let S be an AMI over N with non trivial instruction locations. Observe that the instruction locations of S is non trivial.

Next we state the proposition

(18) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and I be an instruction of S. If for every instruction-location f of S holds $\mathrm{NIC}(I, f) = \{\mathrm{NextLoc}\,f\}$, then $\mathrm{JUMP}(I)$ is empty.

Let N be a set with non empty elements and let I be an instruction of $\mathrm{STC}(N)$. Observe that $\mathrm{JUMP}(I)$ is empty.

Let N be a set and let S be an AMI over N. We say that S is regular if and only if:

(Def. 11) For every instruction type T of S holds AddressParts T is product-like.

Let N be a set. Observe that every AMI over N which is regular is also homogeneous.
We now state the proposition

(19) For every instruction type T of $\mathrm{STC}(N)$ holds $\mathrm{AddressParts}\, T = \{0\}$.

Let N be a set with non empty elements. One can verify that $\mathrm{STC}(N)$ is regular and has explicit jumps and no implicit jumps.

Let N be a set with non empty elements. One can check that there exists an IC-Ins-separated definite non empty non void AMI over N which is standard, regular, halting, realistic, steady-programmed, and programmable and has explicit jumps and no implicit jumps.

Let N be a set with non empty elements, let S be a regular AMI over N, and let T be an instruction type of S. One can check that $\mathrm{AddressParts}\, T$ is product-like.

Let N be a set with non empty elements, let S be a homogeneous AMI over N, and let T be an instruction type of S. Note that $\mathrm{AddressParts}\, T$ has common domain.

Next we state the proposition

(20) Let S be a homogeneous non empty non void AMI over N, I be an instruction of S, and x be a set. Suppose $x \in \mathrm{dom}\, \mathrm{AddressPart}(I)$. Suppose $\prod_{\mathrm{AddressParts}\, \mathrm{InsCode}(I)}(x) =$ the instruction locations of S. Then $(\mathrm{AddressPart}(I))(x)$ is an instruction-location of S.

Let N be a set with non empty elements and let S be an IC-Ins-separated definite non empty non void AMI over N with explicit jumps. Note that every instruction of S has explicit jumps.

Let N be a set with non empty elements and let S be an IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. Observe that every instruction of S has no implicit jumps.

We now state the proposition

(21) Let S be a realistic IC-Ins-separated definite non empty non void AMI over N with non trivial instruction locations and I be an instruction of S. If I is halting, then $\mathrm{JUMP}(I)$ is empty.

Let N be a set with non empty elements, let S be a halting realistic IC-Ins-separated definite non empty non void AMI over N with non trivial instruction locations, and let I be a halting instruction of S. Note that $\mathrm{JUMP}(I)$ is empty.

Let N be a set with non empty elements and let S be an IC-Ins-separated definite non empty non void AMI over N with non trivial instruction locations. One can verify that there exists a finite partial state of S which is non trivial and programmed.

Let N be a set with non empty elements and let S be a standard halting IC-Ins-separated definite non empty non void AMI over N. Observe that every non empty programmed finite partial state of S which is trivial is also unique-halt.

Let N be a set, let S be an AMI over N, and let I be an instruction of S. We say that I is instruction location free if and only if:

(Def. 12) For every set x such that $x \in \mathrm{dom}\, \mathrm{AddressPart}(I)$ holds $\prod_{\mathrm{AddressParts}\, \mathrm{InsCode}(I)}(x) \neq$ the instruction locations of S.

The following two propositions are true:

(22) Let S be a halting realistic IC-Ins-separated definite non empty non void AMI over N with explicit jumps and non trivial instruction locations and I be an instruction of S. If I is instruction location free, then $\mathrm{JUMP}(I)$ is empty.

(23) Let S be a realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and non trivial instruction locations and I be an instruction of S. If I is halting, then I is instruction location free.

Let N be a set with non empty elements and let S be a realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and non trivial instruction locations. One can check that every instruction of S which is halting is also instruction location free.

We now state the proposition

(24) Let S be a standard IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and I be an instruction of S. If I is sequential, then I is instruction location free.

Let N be a set with non empty elements and let S be a standard IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. Observe that every instruction of S which is sequential is also instruction location free.

Let N be a set with non empty elements and let S be a standard halting IC-Ins-separated definite non empty non void AMI over N. The functor $\mathrm{Stop}\,S$ yielding a finite partial state of S is defined as follows:

(Def. 13) $\mathrm{Stop}\,S = \mathrm{il}_S(0) \dot{\longmapsto} \mathbf{halt}_S$.

Let N be a set with non empty elements and let S be a standard halting IC-Ins-separated definite non empty non void AMI over N. Note that $\mathrm{Stop}\,S$ is lower, non empty, programmed, and trivial.

Let N be a set with non empty elements and let S be a standard realistic halting IC-Ins-separated definite non empty non void AMI over N. One can check that $\mathrm{Stop}\,S$ is closed.

Let N be a set with non empty elements and let S be a standard halting steady-programmed IC-Ins-separated definite non empty non void AMI over N. One can verify that $\mathrm{Stop}\,S$ is autonomic.

We now state three propositions:

(25) For every standard halting IC-Ins-separated definite non empty non void AMI S over N holds $\mathrm{card}\,\mathrm{Stop}\,S = 1$.

(26) Let S be a standard halting IC-Ins-separated definite non empty non void AMI over N and F be a pre-Macro of S. If $\mathrm{card}\,F = 1$, then $F = \mathrm{Stop}\,S$.

(27) For every standard halting IC-Ins-separated definite non empty non void AMI S over N holds $\mathrm{LastLoc}\,\mathrm{Stop}\,S = \mathrm{il}_S(0)$.

Let N be a set with non empty elements and let S be a standard halting IC-Ins-separated definite non empty non void AMI over N. One can verify that $\mathrm{Stop}\,S$ is halt-ending and unique-halt.

Let N be a set with non empty elements and let S be a standard halting IC-Ins-separated definite non empty non void AMI over N. Then $\mathrm{Stop}\,S$ is a pre-Macro of S.

4. On the Composition of Macro Instructions

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let I be an element of the instructions of S, and let k be a natural number. The functor $\mathrm{IncAddr}(I,k)$ yielding an instruction of S is defined by the conditions (Def. 14).

(Def. 14)(i) $\mathrm{InsCode}(\mathrm{IncAddr}(I,k)) = \mathrm{InsCode}(I)$,

(ii) $\mathrm{dom}\,\mathrm{AddressPart}(\mathrm{IncAddr}(I,k)) = \mathrm{dom}\,\mathrm{AddressPart}(I)$, and

(iii) for every set n such that $n \in \mathrm{dom}\,\mathrm{AddressPart}(I)$ holds if $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(n) =$ the instruction locations of S, then there exists an instruction-location f of S such that $f = (\mathrm{AddressPart}(I))(n)$ and $(\mathrm{AddressPart}(\mathrm{IncAddr}(I,k)))(n) = \mathrm{il}_S(k + \mathrm{locnum}(f))$ and if $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(n) \neq$ the instruction locations of S, then $(\mathrm{AddressPart}(\mathrm{IncAddr}(I,k)))(n) = (\mathrm{AddressPart}(I))(n)$.

Next we state three propositions:

(28) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I be an element of the instructions of S. Then $\mathrm{IncAddr}(I,0) = I$.

(29) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I be an instruction of S. If I is instruction location free, then $\mathrm{IncAddr}(I,k) = I$.

(30) Let S be a halting standard realistic regular IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. Then $\mathrm{IncAddr}(\mathbf{halt}_S,k) = \mathbf{halt}_S$.

Let N be a set with non empty elements, let S be a halting standard realistic regular IC-Ins-separated definite non empty non void AMI over N with no implicit jumps, let I be a halting instruction of S, and let k be a natural number. Observe that $\mathrm{IncAddr}(I,k)$ is halting.

Next we state several propositions:

(31) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I be an instruction of S. Then $\mathrm{AddressParts}\,\mathrm{InsCode}(I) = \mathrm{AddressParts}\,\mathrm{InsCode}(\mathrm{IncAddr}(I,k))$.

(32) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I, J be instructions of S. Given a natural number k such that $\mathrm{IncAddr}(I,k) = \mathrm{IncAddr}(J,k)$. Suppose $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(x) =$ the instruction locations of S. Then $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(J)}(x) =$ the instruction locations of S.

(33) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I, J be instructions of S. Given a natural number k such that $\mathrm{IncAddr}(I,k) = \mathrm{IncAddr}(J,k)$. Suppose $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(I)}(x) \neq$ the instruction locations of S. Then $\prod_{\mathrm{AddressParts}\,\mathrm{InsCode}(J)}(x) \neq$ the instruction locations of S.

(34) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I, J be instructions of S. If there exists a natural number k such that $\mathrm{IncAddr}(I,k) = \mathrm{IncAddr}(J,k)$, then $I = J$.

(35) Let S be a regular standard halting realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and I be an instruction of S. If $\mathrm{IncAddr}(I,k) = \mathbf{halt}_S$, then $I = \mathbf{halt}_S$.

(36) Let S be a regular standard halting realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and I be an instruction of S. If I is sequential, then $\mathrm{IncAddr}(I,k)$ is sequential.

(37) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and I be an instruction of S. Then $\mathrm{IncAddr}(\mathrm{IncAddr}(I,k),m) = \mathrm{IncAddr}(I,k+m)$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let p be a programmed finite partial state of S, and let k be a natural number. The functor $\mathrm{IncAddr}(p,k)$ yielding a finite partial state of S is defined by:

(Def. 15) $\mathrm{dom}\,\mathrm{IncAddr}(p,k) = \mathrm{dom}\,p$ and for every natural number m such that $\mathrm{il}_S(m) \in \mathrm{dom}\,p$ holds $(\mathrm{IncAddr}(p,k))(\mathrm{il}_S(m)) = \mathrm{IncAddr}(\pi_{\mathrm{il}_S(m)}p,k)$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let F be a programmed finite partial state of S, and let k be a natural number. Note that $\mathrm{IncAddr}(F,k)$ is programmed.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let F be an empty programmed finite partial state of S, and let k be a natural number. Note that $\mathrm{IncAddr}(F,k)$ is empty.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let F be a non empty programmed finite partial state of S, and let k be a natural number. Observe that $\mathrm{IncAddr}(F,k)$ is non empty.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, let F be a lower programmed finite partial state of S, and let k be a natural number. Note that $\mathrm{IncAddr}(F,k)$ is lower.

One can prove the following two propositions:

(38) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and F be a programmed finite partial state of S. Then $\mathrm{IncAddr}(F,0) = F$.

(39) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and F be a lower programmed finite partial state of S. Then $\mathrm{IncAddr}(\mathrm{IncAddr}(F,k),m) = \mathrm{IncAddr}(F,k+m)$.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, let p be a finite partial state of S, and let k be a natural number. The functor $\mathrm{Shift}(p,k)$ yielding a finite partial state of S is defined by the conditions (Def. 16).

(Def. 16)(i) $\mathrm{dom}\,\mathrm{Shift}(p,k) = \{\mathrm{il}_S(m+k); m$ ranges over natural numbers: $\mathrm{il}_S(m) \in \mathrm{dom}\,p\}$, and

(ii) for every natural number m such that $\mathrm{il}_S(m) \in \mathrm{dom}\,p$ holds $(\mathrm{Shift}(p,k))(\mathrm{il}_S(m+k)) = p(\mathrm{il}_S(m))$.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, let F be a finite partial state of S, and let k be a natural number. One can check that $\mathrm{Shift}(F,k)$ is programmed.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, let F be an empty finite partial state of S, and let k be a natural number. One can verify that $\mathrm{Shift}(F,k)$ is empty.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, let F be a non empty programmed finite partial state of S, and let k be a natural number. Note that $\mathrm{Shift}(F,k)$ is non empty.

We now state four propositions:

(40) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a programmed finite partial state of S. Then $\mathrm{Shift}(F,0) = F$.

(41) Let S be a standard IC-Ins-separated definite non empty non void AMI over N, F be a finite partial state of S, and k be a natural number. If $k > 0$, then $\mathrm{il}_S(0) \notin \mathrm{dom}\,\mathrm{Shift}(F,k)$.

(42) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a finite partial state of S. Then $\mathrm{Shift}(\mathrm{Shift}(F,m),k) = \mathrm{Shift}(F,m+k)$.

(43) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a programmed finite partial state of S. Then $\mathrm{dom}\,F \approx \mathrm{dom}\,\mathrm{Shift}(F,k)$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, and let I be an instruction of S. We say that I is IC-good if and only if:

(Def. 17) For every natural number k and for all states s_1, s_2 of S such that $s_2 = s_1 +\cdot (\mathbf{IC}_S \dot{\longmapsto} (\mathbf{IC}_{(s_1)} + k))$ holds $\mathbf{IC}_{\mathrm{Exec}(I,s_1)} + k = \mathbf{IC}_{\mathrm{Exec}(\mathrm{IncAddr}(I,k),s_2)}$.

Let N be a set with non empty elements and let S be a regular standard IC-Ins-separated definite non empty non void AMI over N. We say that S is IC-good if and only if:

(Def. 18) Every instruction of S is IC-good.

Let N be a set with non empty elements, let S be a non void AMI over N, and let I be an instruction of S. We say that I is Exec-preserving if and only if the condition (Def. 19) is satisfied.

(Def. 19) Let s_1, s_2 be states of S. Suppose s_1 and s_2 are equal outside the instruction locations of S. Then $\mathrm{Exec}(I,s_1)$ and $\mathrm{Exec}(I,s_2)$ are equal outside the instruction locations of S.

Let N be a set with non empty elements and let S be a non void AMI over N. We say that S is Exec-preserving if and only if:

(Def. 20) Every instruction of S is Exec-preserving.

We now state the proposition

(44) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and I be an instruction of S. If I is sequential, then I is IC-good.

Let N be a set with non empty elements and let S be a regular standard IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. Observe that every instruction of S which is sequential is also IC-good.

Next we state the proposition

(45) Let S be a regular standard realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and I be an instruction of S. If I is halting, then I is IC-good.

Let N be a set with non empty elements and let S be a regular standard realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. One can verify that every instruction of S which is halting is also IC-good.

One can prove the following proposition

(46) For every non void AMI S over N and for every instruction I of S such that I is halting holds I is Exec-preserving.

Let N be a set with non empty elements and let S be a non void AMI over N. Note that every instruction of S which is halting is also Exec-preserving.

Let N be a set with non empty elements. Note that $\mathrm{STC}(N)$ is IC-good and Exec-preserving.

Let N be a set with non empty elements. Observe that there exists a regular standard IC-Ins-separated definite non empty non void AMI over N which is halting, realistic, steady-programmed, programmable, IC-good, and Exec-preserving and has explicit jumps and no implicit jumps.

Let N be a set with non empty elements and let S be an IC-good regular standard IC-Ins-separated definite non empty non void AMI over N. Observe that every instruction of S is IC-good.

Let N be a set with non empty elements and let S be an Exec-preserving non void AMI over N. One can check that every instruction of S is Exec-preserving.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, and let F be a non empty programmed finite partial state of S. The functor $\mathrm{CutLastLoc}\,F$ yields a finite partial state of S and is defined as follows:

(Def. 21) $\mathrm{CutLastLoc}\,F = F \setminus (\mathrm{LastLoc}\,F \dot{\longmapsto} F(\mathrm{LastLoc}\,F))$.

One can prove the following two propositions:

(47) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a non empty programmed finite partial state of S. Then $\mathrm{dom}\,\mathrm{CutLastLoc}\,F = \mathrm{dom}\,F \setminus \{\mathrm{LastLoc}\,F\}$.

(48) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a non empty programmed finite partial state of S. Then $\mathrm{dom}\,F = \mathrm{dom}\,\mathrm{CutLastLoc}\,F \cup \{\mathrm{LastLoc}\,F\}$.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, and let F be a non empty trivial programmed finite partial state of S. One can check that $\mathrm{CutLastLoc}\,F$ is empty.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, and let F be a non empty programmed finite partial state of S. Note that $\mathrm{CutLastLoc}\,F$ is programmed.

Let N be a set with non empty elements, let S be a standard IC-Ins-separated definite non empty non void AMI over N, and let F be a lower non empty programmed finite partial state of S. One can verify that $\mathrm{CutLastLoc}\,F$ is lower.

One can prove the following three propositions:

(49) Let S be a standard IC-Ins-separated definite non empty non void AMI over N and F be a non empty programmed finite partial state of S. Then $\mathrm{card}\,\mathrm{CutLastLoc}\,F = \mathrm{card}\,F - 1$.

(50) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, F be a lower non empty programmed finite partial state of S, and G be a non empty programmed finite partial state of S. Then $\mathrm{dom}\,\mathrm{CutLastLoc}\,F$ misses $\mathrm{dom}\,\mathrm{Shift}(\mathrm{IncAddr}(G, \mathrm{card}\,F -' 1), \mathrm{card}\,F -' 1)$.

(51) Let S be a standard halting IC-Ins-separated definite non empty non void AMI over N, F be a unique-halt lower non empty programmed finite partial state of S, and I be an instruction-location of S. If $I \in \mathrm{dom}\,\mathrm{CutLastLoc}\,F$, then $(\mathrm{CutLastLoc}\,F)(I) \neq \mathbf{halt}_S$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, and let F, G be non empty programmed finite partial states of S. The functor $F; G$ yielding a finite partial state of S is defined as follows:

(Def. 22) $F; G = \mathrm{CutLastLoc}\,F +\cdot \mathrm{Shift}(\mathrm{IncAddr}(G, \mathrm{card}\,F -' 1), \mathrm{card}\,F -' 1)$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, and let F, G be non empty programmed finite partial states of S. One can check that $F; G$ is non empty and programmed.

One can prove the following proposition

(52) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, F be a lower non empty programmed finite partial state of S, and G be a non empty programmed finite partial state of S. Then $\mathrm{card}(F; G) = (\mathrm{card}\,F + \mathrm{card}\,G) - 1$ and $\mathrm{card}(F; G) = (\mathrm{card}\,F + \mathrm{card}\,G) -' 1$.

Let N be a set with non empty elements, let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, and let F, G be lower non empty programmed finite partial states of S. One can verify that $F; G$ is lower.

One can prove the following four propositions:

(53) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and F, G be lower non empty programmed finite partial states of S. Then $\mathrm{dom}\,F \subseteq \mathrm{dom}(F; G)$.

(54) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and F, G be lower non empty programmed finite partial states of S. Then $\mathrm{CutLastLoc}\,F \subseteq \mathrm{CutLastLoc}\,F; G$.

(55) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N and F, G be lower non empty programmed finite partial states of S. Then $(F; G)(\mathrm{LastLoc}\,F) = (\mathrm{IncAddr}(G, \mathrm{card}\,F -' 1))(\mathrm{il}_S(0))$.

(56) Let S be a regular standard IC-Ins-separated definite non empty non void AMI over N, F, G be lower non empty programmed finite partial states of S, and f be an instruction-location of S. If $\mathrm{locnum}(f) < \mathrm{card}\,F - 1$, then $(\mathrm{IncAddr}(F, \mathrm{card}\,F -' 1))(f) = (\mathrm{IncAddr}(F; G, \mathrm{card}\,F -' 1))(f)$.

Let N be a set with non empty elements, let S be a regular standard realistic halting steady-programmed IC-Ins-separated definite non empty non void AMI over N with no implicit jumps, let F be a lower non empty programmed finite partial state of S, and let G be a halt-ending lower non empty programmed finite partial state of S. Note that $F; G$ is halt-ending.

Let N be a set with non empty elements, let S be a regular standard realistic halting steady-programmed IC-Ins-separated definite non empty non void AMI over N with no implicit jumps, and let F, G be halt-ending unique-halt lower non empty programmed finite partial states of S. Note that $F; G$ is unique-halt.

Let N be a set with non empty elements, let S be a regular standard realistic halting steady-programmed IC-Ins-separated definite non empty non void AMI over N with no implicit jumps, and let F, G be pre-Macros of S. Then $F; G$ is a pre-Macro of S.

Let N be a set with non empty elements, let S be a realistic halting steady-programmed IC-good Exec-preserving regular standard IC-Ins-separated definite non empty non void AMI over N, and let F, G be closed lower non empty programmed finite partial states of S. Note that $F; G$ is closed.

We now state several propositions:

(57) Let S be a regular standard halting realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps. Then $\mathrm{IncAddr}(\mathrm{Stop}\,S, k) = \mathrm{Stop}\,S$.

(58) For every standard halting IC-Ins-separated definite non empty non void AMI S over N holds $\mathrm{Shift}(\mathrm{Stop}\,S, k) = \mathrm{il}_S(k) \longmapsto \mathbf{halt}_S$.

(59) Let S be a regular standard halting realistic IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and F be a pre-Macro of S. Then F; $\mathrm{Stop}\,S = F$.

(60) Let S be a regular standard halting IC-Ins-separated definite non empty non void AMI over N and F be a pre-Macro of S. Then $\mathrm{Stop}\,S$; $F = F$.

(61) Let S be a regular standard realistic halting steady-programmed IC-Ins-separated definite non empty non void AMI over N with no implicit jumps and F, G, H be pre-Macros of S. Then $(F; G); H = F; (G; H)$.

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